AF 10/28/05 JFW

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 15

Application Number	10/706,162
Filing Date	Nov. 12, 2003
First Named Inventor	Farid Nemati
Art Unit	2815
Examiner Name	Jerome Jackson Jr.
Attorney Docket Number	C-028

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name			
Signature	Hark Chan		
Printed name	Hark Chan		
Date	Oct 18, 2005	Reg. No.	35,477

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Hark Chan		
Typed or printed name	Hark Chan	Date	Oct 18, 2005

PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 250

Complete if Known	
Application Number	10/706,162
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First Named Inventor	Farid Nemati
Examiner Name	Jackson Jr., Jerome
Art Unit	2815
Attorney Docket No.	C-028

METHOD OF PAYMENT (check all that apply)

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☑ Deposit Account Deposit Account Number: 50-2538 Deposit Account Name: H. C. Chan

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ Extra Claims x Fee ($) _____ = Fee Paid ($) _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims _____ - 3 or HP = _____ Extra Claims x Fee ($) _____ = Fee Paid ($) _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ Extra Sheets _____ / 50 = _____ Number of each additional 50 or fraction thereof (round up to a whole number) x Fee ($) _____ = Fee Paid ($) _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): appeal brief	250

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 35,477	Telephone (408) 597-3644
Name (Print/Type)	H. C. Chan		Date Oct 18, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nemati, et al.	Examiner:	Jerome Jackson Jr.
Serial No.:	**10/706,162**	Group Art Unit:	2815
Filed:	Nov. 12, 2003	Docket No.:	C-028
Title:	THYRISTOR CIRCUIT AND APPROACH FOR TEMPERATURE STABILITY		

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant submits the present appeal brief, in triplicate, within two months of the mailing of the previous filed Notice of Appeal. The commissioner is hereby authorized to charge $250 for filing this appeal brief, or any other fees which may be required, to deposit account 50-2538.

TABLE OF CONTENTS

(1) Real party in interest

The present application has been assigned by all the inventors to T-RAM, Inc. Thus, the real party in interest is T-RAM, Inc.

(2) Related appeals and interferences

There are no related appeals and interferences.

(3) Status of claims

Twenty eight claims were originally filed and claim 28 has been cancelled. Claims 1-27 are now pending. Claims 1-6, 15, 19-22, 24 and 26 are rejected and claims 4, 7, 16-18, 23, 25 and 27 are objected to. The rejection of claims 1-6, 15, 19-22, 24 and 26 is appealed.

(4) Status of amendments

No amendment has been filed subsequent to final rejection.

(5) Summary of invention

The present invention is directed to a semiconductor device comprising a thyristor that can accept an external signal for controlling the holding current or forward blocking voltage of the thyristor as a function of temperature (e.g., see page 7, lines 1-5 of the specification). The thyristor has a first and a second base region (e.g., P-base 114 and N-base 116 in Fig. 2A). The external signal is generated by a control circuit (e.g., circuit 190 of Fig. 2A) and is coupled to one of the base regions of the thyristor. In one embodiment, the semiconductor device has two control ports (e.g., ports 122 and 124 of Fig. 2A). One of the control ports (e.g., port 124) is disposed above a base region (e.g., N-base 116) and can couple the external signal

(generated by circuit 190) to the base region. The other control port (e.g., port 122) can coupled another signal to the other base region.

The above described semiconductor device can be used to form a memory device (e.g., page 10, lines 28-30).

(6) Issues

The issue presented for review is whether claims 1-6, 15, 19-22, 24 and 26 are unpatentable over Nemati (U.S. Pat. No. 6,462,359) under 35 U.S.C. 102(b) and 35 U.S.C. 103(a).

(7) Grouping of claims

Claims 3-5 contain at least one additional element (temperature sensing circuit) that is not recited in claims 1-2, 6, 15, 19-22, 24, and 26. Claims 3-5 do not stand and fall together with the other rejected claims.

(8) Arguments

(A) Claims 1-2, 6, 15, 19-22, 24 and 26

(1) The External Signal Relied Upon By The Examiner Is Not Coupled to A Base Region Of The Thyristor

The language in claim 1 is representative of a claim element in dispute in this appeal: "a second control port configured and arranged for receiving a second signal generated outside of the thyristor for coupling the second signal at least to the second base region, the second signal being adapted to control holding current or forward blocking voltage of the thyristor as a function of temperature."

On page 2 of the Final Office Action, the Examiner wrote:

"Applicant's arguments filed 3/9/05 have been fully considered but they are not persuasive. Arguments on page 8 of the remarks that the Nemati device cannot be configured and arranged for receiving a signal outside of the thyristor are unconvincing in view of column 7 lines 35-40 of Nemati. Applicant quotes the relevant part of the description of figure 8. There is no evidence that Nemati cannot function in the manner claimed and it is applicant's burden to prove otherwise."

The sentences in Nemati relying upon by the above quote in the Office Action are as follows:

"Alternatively, the gate of the NMOSFET can be independently controlled rather than being connected to the p-base. Other embodiments regarding the use of a FET in combination with a thyristor can be found in U.S. Pat. No. 4,323,793, which is fully incorporated herein by reference." (Nemati col. 7, lines 35-40)

As explained below, these sentences in Nemati do not teach that the signal applied to the gate of the NMOSFET is **coupled to the second base region**, as recited in claim 1.

The function of the NMOSFET is described in Nemati as follows:

"FIG. 8 shows another example embodiment of the present invention in which an NMOSFET 850 is used to provide a current shunt between anode 812 and n-base 814 of a capacitively-coupled thyristor 800. The source, drain and gate of the NMOSFET are electrically connected to the anode, n-base, and p-base of the thyristor, respectively, when the thyristor is in the forward conducting state, the voltage difference between the gate and source of the NMOSFET is relatively small (such as 0.1V to 0.2V). Therefore, the NMOSFET passes only a very small current and the holding current of the thyristor is acceptably low. When the thyristor is in the forward blocking state, the voltage difference between the gate and source of the NMOSFET is very high (almost equal to the anode to cathode voltage of the thyristor) and the NMOSFET has a small resistance. This approach provides a strong shunt between the anode and n-base of the thyristor, and provides high stability for the blocking state of the thyristor against high temperature and disturbances." (col. 7, lines 17-35)

The above description shows that changes in gate-source voltage of the NMOSFET can affect the current between the anode 812 (which is connected to the source of the NMOSFET)

and n-base 814 (which is connected to the drain of the NMOSFET). As a result, a shunting effect between the anode and n-base of the thyristor can be provided by the NMOSFET. In this description, the gate of the NMOSFET is coupled to the thyristor and thus the gate signal is not externally provide.

The Examiner seems to argue that the statement in col. 7, lines 35-37, of Nemati ("the gate of the NMOSFET can be independently controlled rather than being connected to the p-base") provide the teaching or suggestion for an externally provided gate signal. Assuming that the gate signal can be externally provided, that signal is used to **control the resistance between the source and drain of the NMOSFET**. This is significantly different from the requirement of claim 1 that the second control port is for "coupling the second signal at least to the **second base region**" of the **thyristor**. The Examiner did not point to any disclosure in Nemati that teaches or suggests this limitation of claim 1.

(2) Nemati Does Not Disclose An External Signal For Controlling The Holding Current or Forward Block Voltage As A Function of Temperature

In the above quoted description of Fig. 8 of Nemati, the gate voltage varies as follows:

> "[W]hen the thyristor is in the forward conducting state, the voltage difference between the gate and source of the NMOSFET is relatively small (such as 0.1V to 0.2V). Therefore, the NMOSFET passes only a very small current and the holding current of the thyristor is acceptably low. When the thyristor is in the forward blocking state, the voltage difference between the gate and source of the NMOSFET is very high (almost equal to the anode to cathode voltage of the thyristor) and the NMOSFET has a small resistance." (col. 7, lines 22-31)

Thus, this description indicates that the gate-to-source voltage **varies with the state** of the thyristor (forward conducting versus forward blocking states). Even assuming that the gate-to-source voltage can be externally applied, there is no teaching or suggestion that it is for **controlling the holding current or forward block voltage as a function of temperature**.

In view of the significant differences between the claim invention and Nemati, claims 1-2, 6, 15, 19-22, 24, and 26 are patentable over Nemati.

(B) Claims 3-5

Claims 3-5 further recites a "temperature sensing circuit." This element offers another distinction between the claims and Nemati, thus claims 3-5 should not stand and fall with other rejected claims. In the Final Office Action, the Examiner states:

> "Arguments regarding claim 3 are likewise unconvincing as "a temperature sensing circuit" is broad, the functional language is not structurally distinguishing over Nemati, and the device of "Nemati "provides high stability for the blocking state of the thyristor against high temperature (col. 7 lines 34-35) and "alternatively, the gate of the NMOSFET can be independently controlled" i.e., coupled to an outside "circuit" which in this case should be a temperature sensing circuit as the purpose is to "provide high stability ... against high temperature." Claims 4-5 likewise recite functional language and do not structurally distinguish over Nemati."

The Examiner seems to rely on the quoted statement in Nemati of "provide high stability for the blocking state of the thyristor against high temperature and disturbances" (col. 7, lines 33-35) to argue that it discloses the "temperature sensing circuit" of claim 3. The connection between current, temperature and stability is described in the Summary of Nemati as follows: "A current shunt region is configured and arranged to shunt low-level current between the emitter region and the adjacent base region in a manner that improves the **stability** of the semiconductor device under operating conditions including **high temperature**, voltage, light, noise and other disturbances." (col. 2, lines 60-65; emphasis added). Thus, Nemati teaches that a **benefit** of a current shunt is to improve stability (including temperature). However, there is no teaching and suggestion that the signal of the gate of the NMOSFET is a function of temperature.

Claim 3 recites a "semiconductor device" which "includes a temperature sensing circuit electrically coupled to the thyristor and configured and arranged to apply the second signal to the second control port as a function of the temperature of the thyristor." Based on

the above analysis, Nemati does not teach or suggest a "temperature sensing circuit." Thus, claims 3-5 are patentable over Nemati.

Conclusion

It is believed that all grounds of rejection have been satisfactorily answered. The allowance of the rejected claims is respectfully urged.

The commissioner is hereby authorized to charge $250 for filing this appeal brief, or any other fees which may be required, to deposit account 50-2538.

October 18, 2005

Respectfully Submitted

H. C. Chan
Reg. No. 35, 477

APPENDIX

1. A semiconductor device comprising:

a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region; and

a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region, the second signal being adapted to control holding current or forward blocking voltage of the thyristor as a function of temperature.

2). The semiconductor device of claim 1, further comprising:

a circuit arrangement electrically coupled to the second control port and configured and arranged to apply the second signal to the second control port.

3. The semiconductor device of claim 2, wherein the circuit arrangement includes a temperature sensing circuit electrically coupled to the thyristor and configured and arranged to apply the second signal to the second control port as a function of the temperature of the thyristor.

4. The semiconductor device of claim 2, wherein the second signal applied by the temperature sensing circuit is adapted to increase bipolar gains of the thyristor when the temperature of the thyristor is below a selected threshold.

5. The semiconductor device of claim 4, wherein the selected threshold is a temperature at which the holding current of the thyristor would exceed a design holding current value.

6. A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state; and

a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor.

7. The memory device of claim 6, further comprising a reference thyristor, the first circuit being configured and arranged to detect the failure condition from the reference thyristor.

8. The memory device of claim 7, wherein the reference thyristor is configured and arranged to exhibit temperature-responsive failure prior to the at least one thyristor as the operating temperature of the memory device varies from a design operating temperature thereof.

9. The memory device of claim 8, wherein the reference thyristor is configured and arranged to fail at a lower temperature than the at least one thyristor as the operating temperature increases above the design operating temperature.

10. The memory device of claim 8, wherein the reference thyristor is configured and arranged to fail at a higher temperature than the at least one thyristor as the operating temperature decreases below the design operating temperature.

11. The memory device of claim 6, further comprising a plurality of memory cells, each memory cell including a thyristor, wherein the first circuit further comprises:

a first reference memory cell including a thyristor and adapted to store a data "zero" and to fail to retain the data "zero" as a function of the conductance state of the thyristor in the first reference memory cell before other memory cells in the memory device fail data "zero";

a second reference memory cell including a thyristor and adapted to store a data "one" and to fail to retain the data "one" as a function of the conductance state of the thyristor in the second reference memory cell before other memory cells in the memory device fail data "one"; and

the second circuit being adapted to apply the second signal to the second control port as a function of at least one of the first and second reference memory cells failing to retain data.

12. The memory device of claim 11, wherein an emitter of the thyristor in the first reference memory cell is coupled to a reference voltage signal that is greater than a reference voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of memory cells.

13. The memory device of claim 11, wherein an emitter of the thyristor in the first reference memory cell is coupled to a reference voltage signal that is less than a reference voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of memory cells.

14. The memory device of claim 11, wherein each memory cell includes a pass device coupled to an emitter region of the respective thyristor, each pass device exhibiting leakage, the pass device in the second reference thyristor memory cell being adapted to leak relatively more current than the pass devices in the plurality of memory cells such that the second reference memory cell fails to retain data before the plurality of memory cells fail to retain data.

15. The memory device of claim 6, wherein the second control port and the second base region are configured and arranged such that the second signal increases carrier depletion in the second base region.

16. The memory device of claim 6, wherein the second control port extends over a junction between the second base region and the second emitter region.

17. The memory device of claim 16, wherein the second circuit is adapted to capacitively couple the second signal to the second emitter region for accumulating carriers therein.

18. The memory device of claim 6, wherein the second control port extends over a junction between the first and second base regions.

19. A semiconductor device comprising:

a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions, the thyristor body being maintained in a conductance state as a function of holding current; and

a control circuit configured and arranged for applying a signal to at least one of the base regions for controlling the holding current or forward blocking voltage as a function of temperature, the signal being generated outside of the thyristor.

20. The semiconductor device of claim 19, wherein the thyristor is a thin capacitively-coupled thyristor.

21. The memory device of claim 6, wherein the thyristor is a thin capacitively-coupled thyristor.

22. The semiconductor device of claim 1, wherein the thyristor is a thin capacitively-coupled thyristor.

23. The semiconductor device of claim 1, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.

24. The semiconductor device of claim 1, wherein one of the base regions includes material having defects in a depletion region facing the second control port.

25. The memory device of claim 6, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.

26. The memory device of claim 6, wherein one of the base regions includes material having defects in a depletion region facing the second control port.

27. The semiconductor device of claim 19 further comprising a second control port, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.